

RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, DECEMBER 2017

FIRST YEAR [BATCH 2017-20]

COMPUTER SCIENCE (Honours)

Date : 12/12/2017

Time : 11 am – 3 pm

Paper : I

Full Marks : 75

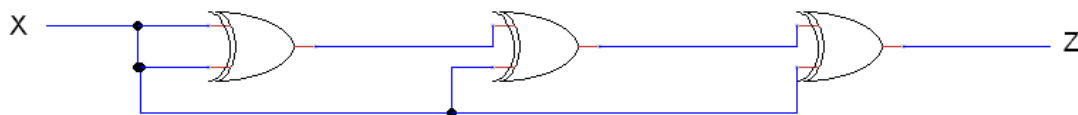
(Use a separate Answer book for each group)

Group – A

Answer **any one** question from **Question Nos. 1 & 2:**

1 X 5

1. a) Show that dual of the exclusive-OR is equal to its complement. Prove or disprove whether it is equally true for the exclusive-NOR. 2
- b) Find the output of the following circuit:– 1



- c) Show that $F(A, B, C) = A'BC + AB' + B'C'$ is a universal operation. 2
2. a) Write an algorithm for conversion of decimal integers to integers in radix R where R is not a power of 10. 3
- b) List the first 16 numbers in base 12. Use the letters A and B to represent last two base 12 digits. 2

Answer **any two** questions **Question Nos. 3 to 6:**

2 X 10

3. a) Subtract $(6ABC.5D)_{16}$ from $(701A.6A)_{16}$. 2
- b) Add the hexadecimal numbers E8E5, EFAB and 5F7A. 2
- c) Multiply $(101.01)_2$ by $(111.10)_2$. 2
- d) Add $(-6571)_8$ with $(-3724)_8$ using diminished radix complement representation. 2
- e) Add the following BCD numbers–
1001 and 0101. 2
4. a) i) Define algorithm. 1+3
- ii) State the characteristics of an algorithm. 3
- b) Define machine-level language, assembly level language and high-level language with suitable examples. 3
- c) A 4-bit message 1010 is transmitted using Hamming code and it reaches to the receiver as 1000010. How does receiver correct it? 3
5. a) Given $A = \bar{B} \cdot C + B \cdot \bar{C}$ then show that $C = \bar{A} \cdot B + A \cdot \bar{B}$. 3
- b) Prove that $\overline{\overline{AB} + ABC + A(B + A\bar{B})} = 0$. 5

- c) Show that the function $F = AB + CD + EFG$ can be expressed using all NAND operators. 2
6. a) Simplify the Boolean function using K-map –

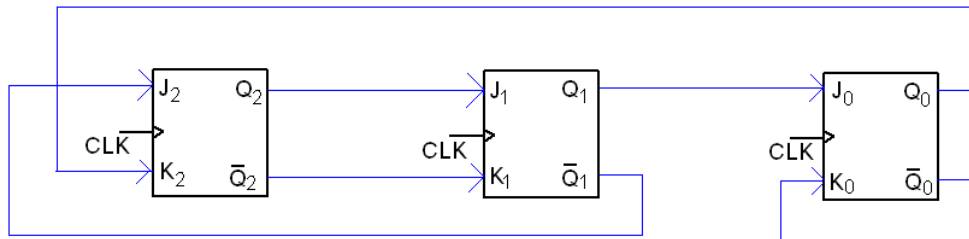
$$F(A, B, C, D) = \sum(0, 2, 3, 4, 5, 8, 10, 11, 12, 13, 14, 15).$$
 4
- b) Use the truth-table technique to establish that the following proposition is tautology
 $\neg \{p \wedge (\neg p \vee q)\} \vee q$. 4
- c) Design a BDD for the function that returns 1 if the inputs have odd parity and 0 if the inputs have even parity. The size of the input is 4. 2

Group – B

Answer **any five** questions **Question Nos. 7 & 14:**

5 X 10

7. a) Why tri-state logic is used in shared bus? 2
- b) What is the limitation of direct-mapped cache? Explain with an example, how it will be improved in set-associative mapped cache. 2+2
- c)



The above synchronous sequential circuit built using JK flip flops is initialized with $Q_2Q_1Q_0 = 000$. Find out the state sequence i.e. $Q_2Q_1Q_0$ for this circuit after two clock cycles. 4

8. a) How does the size of cache block affect the hit ratio? 2
- b) Design a combinational logic circuit which will convert a 3-bit binary number to its 3-bit 2's complement form. 4
- c) Implement a 16 to 1 multiplexer using two 8 to 1 multiplexers. 4
9. a) Realise SR flip-flop using JK flip-flop. 3
- b) Show the control sequence for the execution of the instruction Add R1, R2, R3 in single bus architecture. 5
- c) Find out the minimum number of D flip-flops needed to design a mod-258 counter. 2
10. a) Differentiate between register and direct addressing mode. 2
- b) Which cache mapping technique is free from conflict miss? Explain. 2
- c) Design a synchronous counter which counts the following sequences—
 $0000 \rightarrow 0010 \rightarrow 0100 \rightarrow 0110 \rightarrow 1000 \rightarrow 1010 \rightarrow 1100 \rightarrow 1110 \rightarrow 0000.$ 6

11. a) “Write back protocol of cache memory results unnecessary write operations” – Explain. 2
- b) A computer system uses 16-bit memory address. It has a 2K-byte cache organized in direct mapped manner with 64 bytes per block. Assume that the size of each memory word is 1 byte.
- i) Calculate the number of bits in each of Tag, Block and Word fields of memory address.
- ii) When a programme is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176.
- All the above addresses are shown in decimal. Assume that cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or miss. Also find the hit ratio. 3+4
- c) What is the extra function done by a universal shift register than a bidirectional shift register? 1
12. a) Consider a hard disk with 16 recording surfaces (0 – 15) having 16384 cylinders (0 – 16383) and each cylinder contains 64 sectors (0 – 63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is <cylinder no., surface no., sector no.>. A file of size 42797 KB is stored in the disk and the starting disk location of the file is <1200,9,40>. What is the cylinder number of the last sector of the file, if it is stored in contiguous manner? 5
- b) What is race-around condition? How does master-slave flip-flop avoid it? 3+2
13. a) Multiply -9_{10} and -4_{10} using Booth’s algorithm. 4
- b) Design a 4-bit Johnson counter. 4
- c) Why do we need various addressing modes? 2
14. a) Compare and contrast between CISC and RISC. 3
- b) Explain how Von Neumann architecture is different from Harvard architecture. 2
- c) A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of D flip-flop is set to logic one and the output of JK flip-flop is cleared. What is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when flip-flops are connected to a common clock and five clock pulses are applied? 5

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